Code.No: 07A51102 | R07 | SET-1

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
LINEAR & DIGITAL IC APPLICATIONS
(COMMON TO BME, E.CONT.E, ETM, E.COMP.E)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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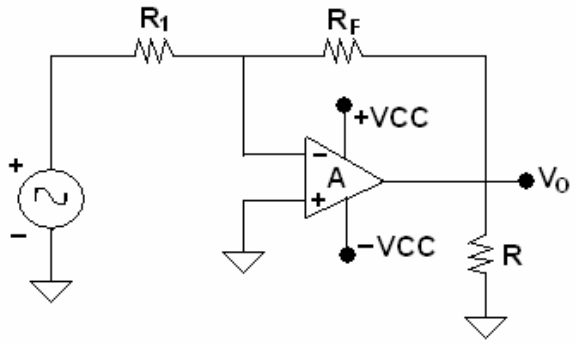
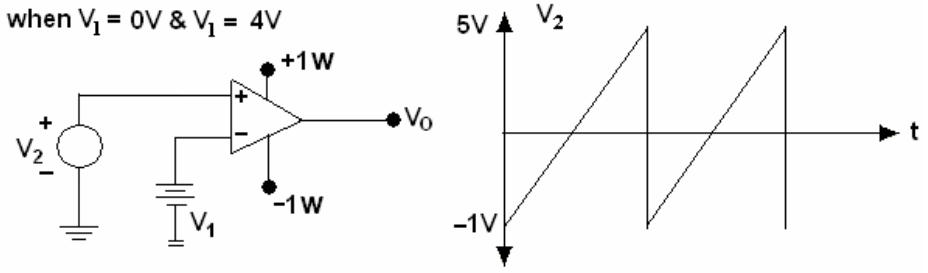
1.a) What is an electrical noise? What precautions can be taken to minimize the effect of noise on an op-amp circuit?

b) Given $R_1 = 100\ \Omega$ and $R_F = 4.7k\Omega$. What is the maximum possible output offset voltage V_{oo}? The op-amp is LM307 with V_{io} =10 mv and supply voltage $\pm$ 15V as shown in figure. [8+8]



2.a) Explain why do we use two stage op-amplifier as an instrumentation amplifier.

b) Draw the output of the op amp as shown in figure. When $V_1 = 0V$ & $V_1 = 4V$. [4+12]



3. Draw the circuit of the second order low pass filter and derive the gain of the filter and also plot the frequency response. [16]

4.a) Explain the function of each pin of 555 timer.

b) List the important features of 555 timer. [8+8]

5.a) Design a first -order low pass filter so that it has a cut off frequency of 2kHz and pass Band gain of '1'

b) Convert the 2 kHz low pass filter to a cut off frequency of 3kHz in part (a) [8+8]

6. Explain with suitable example how binary multiplication can be performed using shift and add method? [16]

7. Explain following terms:
   a) Logic Levels
   b) Speed of logic circuit
   c) Power dissipation
   d) Noise Margin
   e) Noise immunities. [16]

8. a) With neat circuit diagram explain the working of a 4-bit odd parity generator .

b) Design a 2-digit binary multiplication circuit? [6+5+5]

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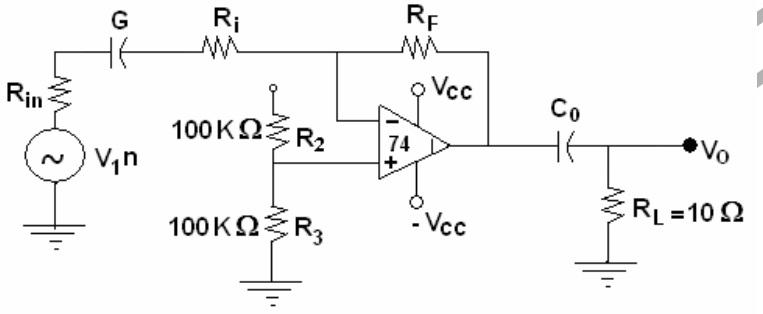
1.a) List out the merits and limitations of integrated circuit technology?
b) Explain the input offset current and input bias current with op-Amps. [8+8]

2.a) What are the limitations of an ordinary op-amp differentiator?
b) The inverting amplifier with a single supply is shown in figure $R_{in} = 50\Omega$, $R_4 = 10k\Omega$, $R_2 = R_3 = R_F = 100k\Omega$ and $C_i = C_0 = 0.1\mu F$. Determine the BW of amplifier. Also determine the maximum ideal output voltage swing. [4+12]



3.a) Design a Band pass filter so that f_c = 1kHz, Q = 3 and A_F = 10.
b) Draw the frequency response. [8+8]

4.a) With neat diagram explain the dual slope type A/D converter?
b) Compare successive approximation type \& single slope ADC? [8+8]

5. If f_s = 100 KHz, the voltage to frequency transfer coefficient of VCO, K_v = 2mHz/v, f_0 the VCO frequency is 5MHZ and N=100 in the frequency multiplier what is the dc voltage at lock? [16]

6. Implement the following functions using a multiplexer:
a) F (A, B, C) = $\sum m(1,3,5,6)$
b) F (A, B, C) = $\sum m(0,1,3,4,8,9,15)$ [16]

7. Explain the MOS and CMOS logic families and different CMOS characteristics. [16]

8.a) With the help of logic diagram of a 4-bit adder/subtractor for adding or subtracting two numbers of arbitrary signs, using 1's complement and explain its working?
b) Design a 4-bit parallel full adder with look ahead carry scheme? [8+8]

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Code.No: 07A51102 | R07 | SET-3

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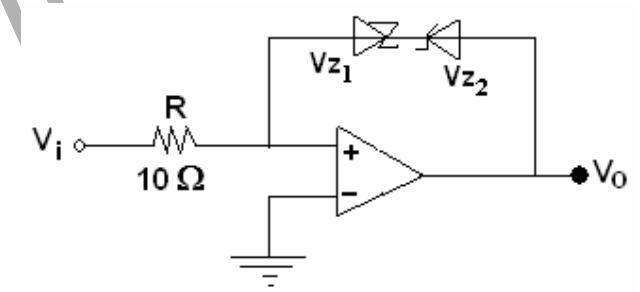
1.a) Why is emitter resistor RE replaced by a constant current bias circuit in differential amplifier stage of an op-amp?
b) Compare and contrast the properties of ideal and practical op-amp. [8+8]

2. For the VCO determine the change in output frequency if V_c is varied between 9V and 11V. Assume that +V = 12V, R_2 = 15kΩ, R_3 = 100 kΩ, R_1 = 0.8 kΩ, and C_1 = 75 Pf. Derive the equations used. [16]

3.a) Distinguish between single slope and dual slope type of A/D converter?
b) What are over sampling converter? [8+8]

4. With neat circuit diagrams explain the following:
a) AND-OR-INVERT gates
b) Open collector TTL 2-input OR gate. [16]

5.a) With a circuit diagram and waveform explain the operation of an inverting and non-inverting comparators.
b) For the circuit as shown in figure draw the output wave form, given V_i = 100mV peak sine wave at 100Hz, R = 1kΩ and V_r = V_z = 6.2V and supply voltage is $\pm$ 12V. [8+8]



6.a) Derive the expression of the lock-in range.
b) Derive the expression of the capture range. [8+8]

7. With the help of neat diagram and truth table explain BCD to 7-segment decoder. [16]

8.a) What is meant by a transparent latch?
b) Convert a D-FF to a JK-FF, using extra NAND gates, if required.
c) Explain the function of preset and clear inputs in flip-flop.
d) Why S=R=1 not permitted in SR-Flip-Flop. [16]

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Code.No: 07A51102 | R07 | SET-4

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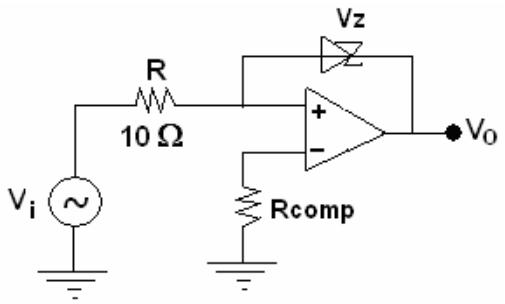
1.a) How many bits are required to design a DAC, that can have a resolution of 5mv? The ladder has +8V full scale?
b) How many resisters are required for an 8-bit weighted resister DAC? What are the resistance values, assuming the smallest resistance is R? [16]

2. Explain the following terms:
a) Floating input
b) Active and passive pull-up
c) Open collector outputs
d) Unused points. [16]

3. Design a BCD to gray code converter using:
a) 8:1 multiplexer.
b) BCD to decimal decoder and NAND gates.
c) NAND gates only. [16]

4. Write short notes on the following:
a) Level triggering.
b) Edge triggering.
c) Pulse triggering
d) Explain the RS flip-flop using NAND gates? [8+8]

5.a) Describe the limitations of op-amp as a comparator.
b) In the as shown in figure determine the output voltage swing and draw the output waveform given V_i = 500mV peak 100Hz sine wave, R = 100 Ω , V_z = 6.2, V_1, V_D = 0.7V and supply voltages = ± 15V. [8+8]

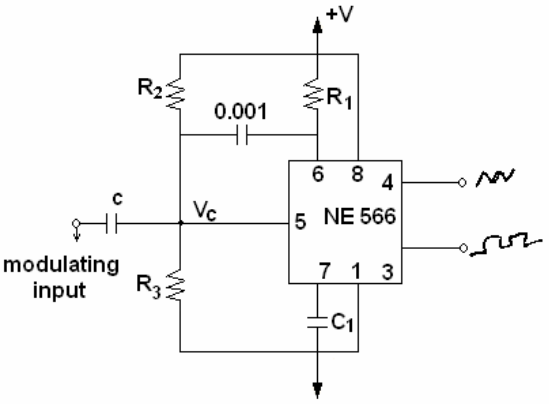


6.a) Derive that the period of a triangular wave is T= 4 R_1 C_1 (R_2/R_3).

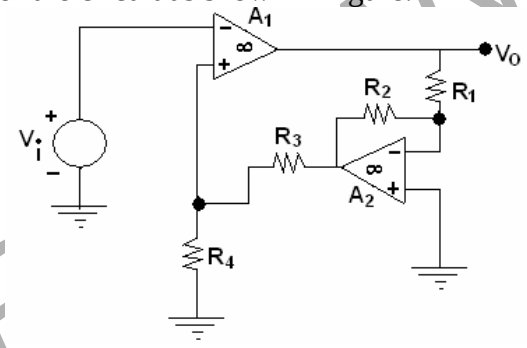
b) In the circuit as shown in figure +V = +12V, R_2 = 1.5 kΩ, R_1 = R_3 = 10 kΩ & C_1 = 0.001 μ f.

i) Determine the nominal frequency of the output waveforms.

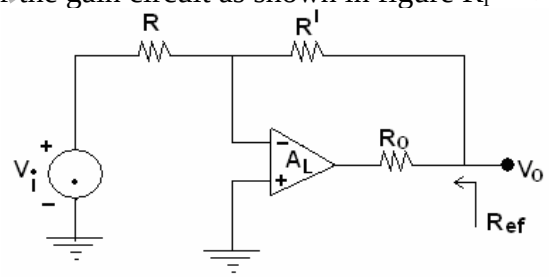
ii) Draw the square wave output waveform if the modulating input is a sine wave. [16]



7.a) Calculate v_0 /$v_1$for the circuit as shown in figure.



b) Calculate Y_{of} for the gain circuit as shown in figure $R_i = \infty$ [8+8]



8.a) A system uses a 12-bit word to represent the input signal of the maximum peak - to-peak voltage at the input is set to 5V,find the resolution of the system and the dynamic range.

b) Explain the characteristics of an n-bit weighted resistor D/A converter? [8+8]

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